CLAIMS

WHAT IS CLAIMED IS:

1. A combined sidetone and hybrid balance apparatus comprising:

at least one filter, the at least one filter having an input and an output;

a combiner having at least a first input and a second input, the second input coupled to the output of the at least one filter, the combiner for combining the at least a first input and a second input to produce an output;

a first switch coupling a first input signal to the first input of the combiner in a first mode of operation, and coupling a second input signal to the first input of the combiner in a second mode of operation;

a second switch coupling the output of the combiner to a first output in the first mode of operation, and coupling the input of the at least one filter to the first output in the second mode of operation;

a third switch coupling a second input signal to the input of the at least one filter in the first mode of operation, and coupling the first input signal to the input of the at least one filter in the second mode of operation; and

a fourth switch coupling the input of the at least one filter to a second output in the first mode of operation, and coupling the output of the combiner to the second output in the second mode of operation.

2. The combined sidetone and hybrid balance apparatus of claim 1 wherein the at least one filter is a digital filter.

3. The combined sidetone and hybrid balance apparatus of claim 1 wherein the at least one filter is a finite element response (FIR) filter.

4. The combined sidetone and hybrid balance apparatus of claim 1 wherein the at least one filter is a finite element response (FIR) filter with at least three taps.

5. The combined sidetone and hybrid balance apparatus of claim 1 wherein the at least one filter uses a first predetermined set of filter coefficients in the first mode of operation, and a second predetermined set of filter coefficients in the second mode of operation.

6. The combined sidetone and hybrid balance apparatus of claim 5 wherein the first predetermined set of filter coefficients and the second predetermined set of filter coefficients are different.

7. The combined sidetone and hybrid balance apparatus of claim 1 wherein the combining comprises one of at least adding the first input to the second input, adding the first input to the negative of the second input, and subtracting the second input from the first input.

8. The combined sidetone and hybrid balance apparatus of claim 1 wherein the functionality is contained within a single integrated circuit device.

9. A combined sidetone and hybrid balance apparatus comprising:

a first signal path carrying a first signal;

a second signal path carrying a second signal;

a mode input having at least a first state and a second state;

a reconfigurable filter for modifying at least one of the first signal and the second signal; and

wherein the apparatus generates a sidetone signal in the first signal by combining at least a portion of the second signal with the first signal when the mode input is in the first state, and cancels an echo in the second signal by subtracting at least a portion of the first signal from the second signal when the mode input is in the second state.

10. The apparatus of claim 9 wherein the signals in the first signal path and the second signal path are digital signals.

11. The apparatus of claim 9 wherein the apparatus is contained within a single integrated circuit.

12. A method of operating a combined sidetone and hybrid balance apparatus, the method comprising:

receiving a first input signal;

receiving a second input signal;

when in a first mode of operation,

filtering the second input signal;

combining the first input signal and the filtered second input signal to produce a combined signal;

transmitting the combined signal on a first output; and

transmitting the second input signal on a second output, and

when in a second mode of operation,

filtering the first input signal;

transmitting the first input signal on the first output;

combining the second input signal and the filtered first input signal to produce a combined signal; and

transmitting the combined signal on the second output.

13. The method of claim 12 wherein the filtering uses a digital filter.

14. The method of claim 12 wherein the filtering uses a finite impulse response filter.

15. The method of claim 12 wherein the filtering uses a finite impulse response filter with at least three taps.

16. The method of claim 12 wherein the at least one filter uses a first predetermined set of filter coefficients in the first mode of operation, and a second predetermined set of filter coefficients in the second mode of operation.

17. The method of claim 16 wherein the first predetermined set of filter coefficients and the second predetermined set of filter coefficients are different.

18. The method of claim 12 wherein the combining comprises one of at least adding the first input to the second input, adding the first input to the negative of the second input, and subtracting the second input from the first input.

19. The method of claim 12 wherein the receiving, filtering, combining, and transmitting are performed within a single integrated circuit device.

20. A method of operating a combined sidetone and hybrid balance apparatus having a first signal path and a second signal path, the method comprising:

Receiving a control signal having at least a first state and a second state;

Configuring an electrical circuit based upon the control signal;

Generating a sidetone signal in the first signal path by adding at least a portion of the signal from the second signal path to the signal in the first signal path if the control signal is in the first state; and

Canceling an echo signal in the second signal path by subtracting from the signal in the second signal path a modified version of the signal in the first signal path if the control signal is in the second state.

21. The method of claim 20 wherein the signals traversing the first signal path and the second signal path are digital signals.

22. The method of claim 20 wherein the method is performed within a single integrated circuit device.